Project 1

Logic Simulator

Georgia Institute of Technology

ECE 6140

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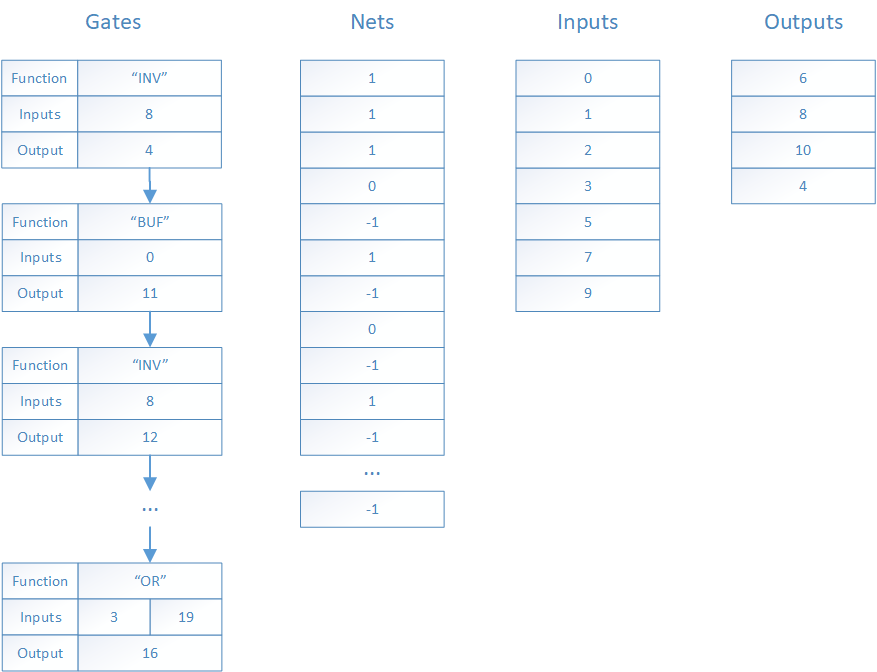
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**Data Structures**

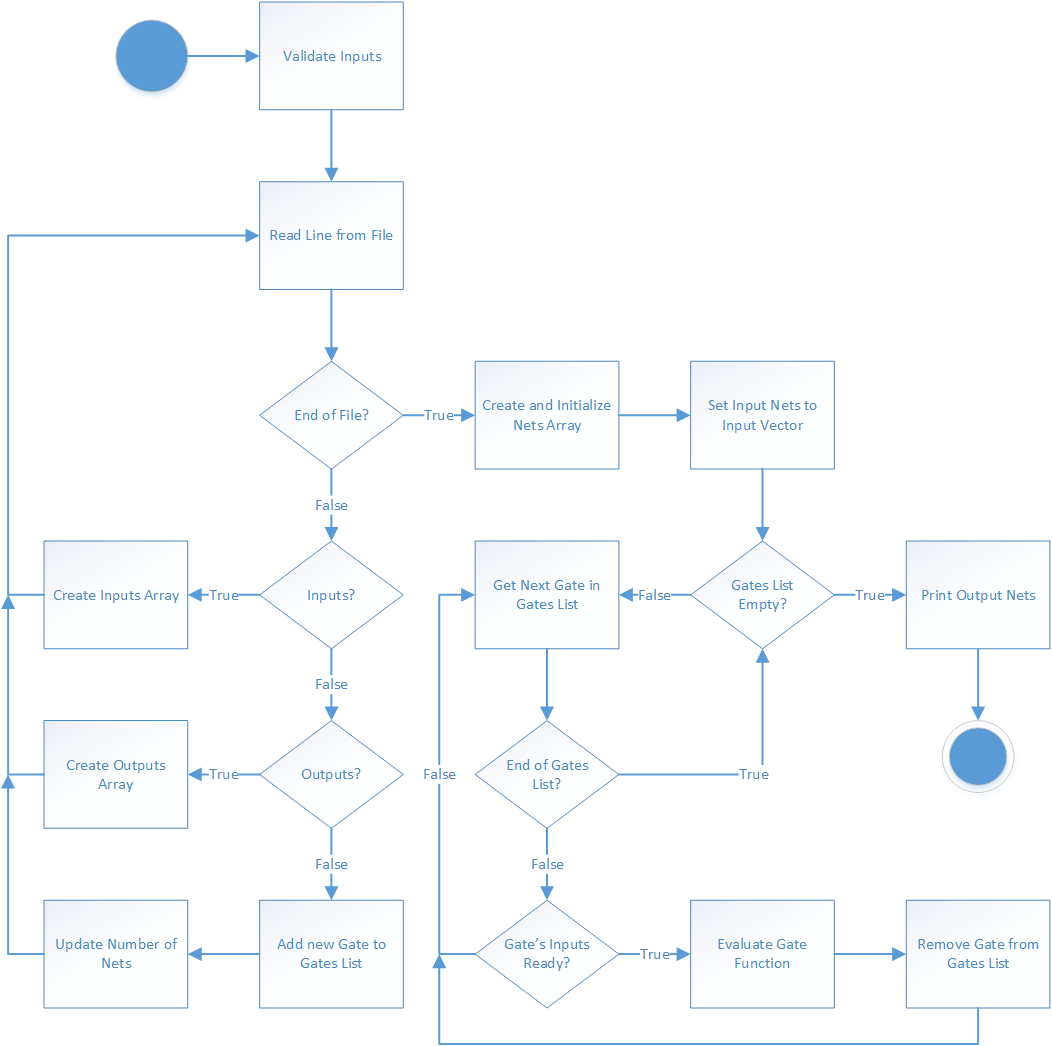
The simulation uses three arrays and one linked list. The “nets” array stores the value of each net as an integer at the index corresponding the net number minus one. The “inputs” array stores the index to the “nets” array of each net that is an input to the circuit. The “outputs” array stores the index to the “nets” array of each net that is an output to the circuit. The “gates” linked list stores a list of nodes that represent logic gates in the circuit. The nodes in the linked list are instances of the Gate class. The Gate class has three data fields. The “function” String stores the type of gate (e.g. “INV”, “BUF”, etc.). The “inputs” array stores the index to the “nets” array of each net that is an input to the gate. The “output” integer stores the index to the “nets” array of the output of the gate. Figure 1 shows a snapshot of these data structures.

**Simulation Flow**

The simulation has two main loops. The first loop parses the input file line by line, and the second loop evaluates the logic gates in the circuit. In each iteration of the first loop, a new instance of the Gate class is created and added to the end of the “gates” linked list. Next, the “nets” array is created and each net is initialized with a value of -1 to indicate that the value is unknown. Then each input net is set to its value in the input vector. In each iteration of the second loop, the next gate in the list of gates is fetched. If all of the inputs to the gate are ready (i.e. none of the nets have a value of -1), then the gate function is evaluated and the output is stored at its index in the “nets” array. The gate is then removed from the list of gates. The second loop will terminate after all gates have been evaluated and the list of gates is empty. Figure 2 shows the flow of the simulator.



**Figure 1.** Snapshot of data structures after parsing the s27 circuit file with an input vector of 1110101.



**Figure 2.** Algorithmic State Machine that describes the flow of the simulator.

**Table 1.** Outputs of Four Test Circuits with Corresponding Inputs

|  |  |  |
| --- | --- | --- |
| Circuit | Input | Output |
| s27 | 1110101 | 1001 |
| 0001010 | 0100 |
| 1010101 | 1001 |
| 0110111 | 0001 |
| 1010001 | 1001 |
| s298f\_2 | 10101010101010101 | 00000010101000111000 |
| 01011110000000111 | 00000000011000001000 |
| 11111000001111000 | 00000000001111010010 |
| 11100001110001100 | 00000000100100100101 |
| 01111011110000000 | 11111011110000101101 |
| s344f\_2 | 101010101010101011111111 | 10101010101010101010101101 |
| 010111100000001110000000 | 00011110000000100001111100 |
| 111110000011110001111111 | 00011100000111011000111010 |
| 111000011100011000000000 | 00001101111001111111000010 |
| 011110111100000001111111 | 10011101111000001001000100 |
| s349f\_2 | 101010101010101011111111 | 10101010101010101101010101 |
| 010111100000001110000000 | 00011110000000101011110000 |
| 111110000011110001111111 | 00011100000111010001111100 |
| 111000011100011000000000 | 00001101111001110010001111 |
| 011110111100000001111111 | 10011101111000001010000100 |